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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/733,289	12/08/2000	Xiao-Chun Mu	884.798US1	2980

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EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/733,289	MU ET AL.	
	Examiner	Art Unit	
	DILINH NGUYEN	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,10-17,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,10-17,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/25/08,4/1/08*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 4/1/08 has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. Pat. 6160311) in view of Jimarez et al. (U.S. Pat. 6407334).

Chen et al. disclose a semiconductor device (cover fig., figs. 4H and 5A) comprising:

a planar heat sink 32a (column 3, lines 30-31);

more than one microelectronic die 31a (fig. 5A), each having an active surface and a back surface, wherein said more than one microelectronic die back surface adjacent to the heat sink;

a patterned adhesive layer 33a disposed between said more than one microelectronic die 31a and the heat sink 32a; and

an encapsulation material 36a (column 3, lines 58-59) disposed on the heat sink and the microelectronic die active surface.

Chen et al. do not explicitly disclose the patterned adhesive layer 33a is a patterned thermally conductive adhesive.

However, Jimarez et al. disclose a patterned thermally conductive adhesive layer 44 (cover fig., column 3, lines 27-28) disposed between a chip 34 and a planar heat sink 46. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Chen et al. by having the patterned thermally conductive adhesive layer disposed between the chip and the heat sink because as taught by Jimarez et al., such the patterned thermally conductive adhesive layer would increase the heat dissipation between the die and the planar heat sink.

3. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al. (U.S. Pat. 6160311) in view of Jimarez et al. (U.S. Pat. 6407334) as applied to claim 1 above, and further in view of Woodward et al. (U.S. Pat. 4731700).

Chen et al. in view of Jimarez et al. substantially disclose all the limitations as claimed above except for a microelectronic package core and wherein the die is disposed within at least one package core opening.

However, Woodward et al. disclose a semiconductor device (fig. 2, column 4, lines 12-24) comprising:

a ceramic member 14 having a first surface and an opposing second surface, the ceramic member having at least one opening defined therein extending from the ceramic member first surface to the ceramic member second surface, where the ceramic member second surface abuts the planar heat sink 12; and

wherein a die 16 is disposed within the ceramic member opening and adjacent the heat sink, the die having an active surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the microelectronic package core and wherein the die is disposed within at least one package core opening as taught by Woodward et al. into the device structure of Chen et al. in view of Jimarez et al. in order to provide an electrical crossover in the area above the die and increase in interconnect density.

4. Claims 1-4 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (U.S. Pat. 5250843) in view of Jimarez et al. (U.S. Pat. 6407334).

Eichelberger discloses a semiconductor device (fig. 1, column 13, lines 51 et seq.) comprising:

a planar heat sink 12 ;

more than one microelectronic die 14, each having an active surface and a back surface, said more than one microelectronic die back surface adjacent to the heat sink;

a thin die attach material 16 disposed between more than one microelectronic die and the heat sink (column 13, lines 64-66); and

an encapsulation material 18 disposed on the heat sink and the die active surface (fig. 1).

Eichelberger does not disclose a thin die attach material 16 is a patterned thermally conductive adhesive layer.

However, Jimarez et al. disclose a patterned thermally conductive adhesive layer 44 (cover fig., column 3, lines 27-28) disposed between a chip 34 and a planar heat sink 46. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Eichelberger by having the patterned thermally conductive adhesive layer disposed between the chip and the heat sink because as taught by Jimarez et al., such the patterned thermally conductive adhesive layer would increase the heat dissipation between the die and the planar heat sink.

- Regarding claim 2, Eichelberger discloses that a build up layer disposed on an upper surface of the encapsulant material (fig. 1).
- Regarding claim 3, Eichelberger discloses that the build up layer comprises at least on conductive trace 20 disposed on the encapsulation material upper surface, wherein a portion of the conductive trace extending through the encapsualation material to contact the microelectronic die active surface (fig. 1).
- Regarding claim 4, Eichelberger discloses that the build up layer further includes at least one dielectric layer 24 disposed on at least a portion of the encapsulation material upper surface and at least on conductive trace, and at least one second conductive trace 26 extending through the dielectric layer to contact the conductive trace (fig. 1).

- Regarding claim 30, Eichelberger discloses that a build-up layer disposed on an upper surface of the encapsulation material 18, wherein the build-up layer comprises at least one conductive trace 20 disposed on the encapsulation material upper surface, wherein a portion of the at least one conductive trace 20 extending through the encapsulation material 18 to contact at least one microelectronic die active surface (fig. 1).

5. Claim 29 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eichelberger (U.S. Pat. 5250843) in view of Jimarez et al. (U.S. Pat. 6407334) as applied to claim 1 above, and further in view of Woodward et al. (U.S. Pat. 4731700).

Eichelberger in view of Jimarez et al. substantially disclose all the limitations as claimed above except for a microelectronic package core and wherein the die is disposed within at least one package core opening.

However, Woodward et al. disclose a semiconductor device (fig. 2, column 4, lines 12-24) comprising:

a ceramic member 14 having a first surface and an opposing second surface, the ceramic member having at least one opening defined therein extending from the ceramic member first surface to the ceramic member second surface, where the ceramic member second surface abuts the planar heat sink 12; and wherein at least one die 16 is disposed within the ceramic member opening and adjacent the heat sink, the die having an active surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have the microelectronic package core and wherein the die is disposed within at least one package core opening

as taught by Woodward et al. into the device structure of Eichelberger in view of Jimarez et al. in order to provide an electrical crossover in the area above the die and increase in interconnect density.

6. Claims 10 and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (U.S. Pat. 6368894) in view of Woodward et al. (U.S. Pat. 4731700).

Shen discloses a semiconductor device (figs. 1-2, column 4, lines 5 et seq.) comprising:

a planar heat sink 33 (column 5, lines 27);

a package core 1 having a first surface 10 and an opposing second surface 14, the package core having at least one opening 11 (fig. 2) defined therein extending from the package core first surface to the package core second surface;

more than one microelectronic die 3 (column 5, lines 30) disposed within at least one package core opening and adjacent the heat sink, each said more than one microelectronic die having an active surface; and

an encapsulation material 34 disposed on the die and in portions of at least one package core opening.

Shen does not disclose the microelectronic package core second surface abuts the heat sink.

However, Woodward et al. disclose a semiconductor device (fig. 2, column 4, lines 12-24) comprising: a ceramic member 14 having a first surface and an opposing second surface, wherein the ceramic member second surface abuts a planar heat sink 12. Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to have the microelectronic package core second surface abuts the heat sink as taught by Woodward et al. into the device structure of Shen in order to provide good heat dissipation for the semiconductor package device.

- Regarding claim 15, Woodward et al. disclose a thickness of the ceramic member 14 is greater than a thickness of the die 16 (fig. 2).
- Regarding claim 16, Shen discloses the package core is a material selected from the group consisting of ceramics or metals (column 4, lines 5-10).

7. Claims 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (U.S. Pat. 6368894) in view of Woodward et al. (U.S. Pat. 4731700) as applied to claim 10 above, and further in view of Eichelberger (U.S. Pat. 5250843).

Shen in view of Woodward et al. substantially disclose all the limitations as claimed above except for a build up layer disposed on an upper surface of the encapsulation material.

However, Eichelberger discloses a semiconductor device (fig. 1, column 13, lines 51 et seq.) comprising: a build up layer disposed on an upper surface of the encapsulation material 18 to provide interconnection pads (column 10, lines 54-57). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Shen in view of Woodward et al. by having the build up layer disposed on an upper surface of the encapsulation material because as taught by Eichelberger, such the build up layer would provide a direct interconnection between integrated circuit chips.

- Regarding claim 12, Eichelberger discloses the build up layer comprises at least on conductive trace 20 disposed on the encapsulation material upper surface, wherein a portion of the conductive trace extending through the encapsualation material to contact the microelectronic die active surface.
- Regarding claim 13, Eichelberger discloses the build up layer further includes at least one dielectric layer 24 disposed on at least a portion of the encapsulation material upper surface and at least on conductive trace, and at least one second conductive trace 26 extending through the dielectric layer to contact the conductive trace.
- Regarding claim 14, Shen discloses the encapsulation (34 and 24) covers the package core first surface.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen (U.S. Pat. 6368894) in view of Woodward et al. (U.S. Pat. 4731700) as applied to claim 10 above, and further in view of Jimarez et al. (U.S. Pat. 6407334).

Shen in view of Woodward et al. substantially disclose all the limitations as claimed above except for a thermally conductive adhesive layer disposed between the microelectronic die and the planar heat sink.

However, Jimarez et al. disclose a patterned thermally conductive adhesive layer 44 (cover fig., column 3, lines 27-28) disposed between a die 34 and a planar heat sink 46. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Shen in view of Woodward et al. by having the patterned thermally conductive adhesive layer disposed between the chip

and the heat sink because as taught by Jimarez et al., such the thermally conductive adhesive layer would increase the heat dissipation between the die and the planar heat sink.

Response to Arguments

Applicant's arguments filed 4/1/08 have been fully considered but they are not persuasive.

The applicant argues that none of references are teaching a patterned thermally conductive adhesive layer disposed between the more than one microelectronic die and the heat sink.

Applicant's arguments have been fully considered but they are not persuasive because Chen et al. disclose a semiconductor device (cover fig., figs. 4H and 5A) comprising:

more than one microelectronic die 31a (fig. 5A), each having an active surface and a back surface, wherein said more than one microelectronic die back surface adjacent to the heat sink;

a patterned adhesive layer 33a disposed between said more than one microelectronic die 31a and the heat sink 32a; and

Chen et al. do not explicitly disclose the patterned adhesive layer 33a is a patterned thermally conductive adhesive.

However, Jimarez et al. disclose a patterned thermally conductive adhesive layer 44 (cover fig., column 3, lines 27-28) disposed between a chip 34 and a planar heat sink 46. Therefore, it would have been obvious to one having ordinary skill in the art at the

time the invention was made to modify the device of Chen et al. by having the patterned thermally conductive adhesive layer disposed between the chip and the heat sink because as taught by Jimarez et al., such the patterned thermally conductive adhesive layer would increase the heat dissipation between the die and the planar heat sink. Moreover, it is noted that claims 1-4 and 29-30 are directed to semiconductor device. The process limitations do not carry weight in a claims drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985) and the word: "patterned" does not carry weight in a claim drawn to structure. Initially, and with respect to claims 1-4 and 29, note that a "product by process" claim is directed to the product per se, no matter how actually made. See In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) and the related case law cited therein which makes it clear that it is the final product *per se* which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe, Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself, *In re Brown,* 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington,* 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.,* 77 F. 2d 274, 279. 26 USPQ 57, 61 (2d. Cir, 1935).

In response to Applicant's argument that there is no motivation to combine the references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it

that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

The Applicant argues that Woodward's chip 16 and heat sink 12 is a layer of molybdenum 12c that is not taught as an adhesive of any type. Rather, item 12c is simply referred to as a part of the heat sink 12.

The Applicant's arguments have been fully considered but they are not persuasive because Woodward's layer 12c0 is an adhesive layer because the bottom surface of chip 160 is soldered to 12c0 (column 5, lines 35-36). The layer 12c0 is between the chip and the heat sink.

In response to Applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case:

Woodward et al. disclose a semiconductor device (fig. 2, column 4, lines 12-24) comprising:

a ceramic member 14 having a first surface and an opposing second surface, the ceramic member having at least one opening defined therein extending from the

ceramic member first surface to the ceramic member second surface, where the ceramic member second surface abuts the heat sink 12; and

wherein at least one die 16 is disposed within the ceramic member opening and adjacent the heat sink, the die having an active surface. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Chen et al. and Jimarez et al. to provide an electrical crossover in the area above the die and increase in interconnect density, as shown by Woodward et al.

In response to Applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case: Jimarez et al. disclose a patterned thermally conductive adhesive layer 44 (cover fig., column 3, lines 27-28) disposed between the at least one chip 34 and a heat sink 46. Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Eichelberger to increase the heat dissipating between the die and the heat sink, as shown by Jimarez et al.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DILINH NGUYEN whose telephone number is (571)272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

5/27/2008

/Theresa T. Doan/
Primary Examiner, Art Unit 2814